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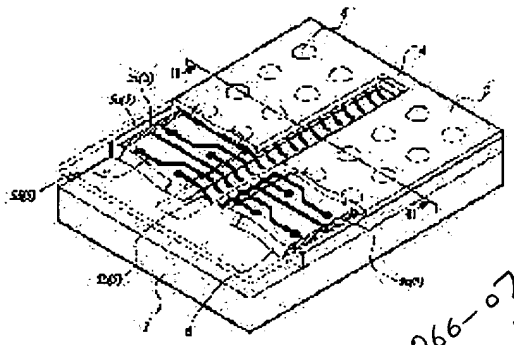
(54) SEMICONDUCTOR DEVICE AND MANUFACTURE THEREFOR

(57)Abstract:
PROBLEM TO BE SOLVED: To facilitate the standardization of in the number of outer leads, the improvement of the performance and the standardization of an input/output terminal arrangement in an area-array-type surface-mounting semiconductor device, wherein a TCP(tape-carrier package) tape is applied.
SOLUTION: A tape substrate 2, wherein copper or copper alloy is a main conductor layer and a gold-plated wiring 5 is provided on the surface, and a semiconductor chip 1 are bonded by a bonding layer 8 composed of an elastic body. Connection is performed to the wiring connecting part on the semiconductor chip 1 by an inner lead part 5b of the wiring 5. In this semiconductor device, a common wiring part 5c, which is grounded or held at a power supply potential, is provided in the wiring 5. A lead wiring part 5d, which is connected directly to the inner lead 5b from the common wiring part 5c, without going through a land part 5a for an external electrode, is provided.



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CLAIMS

[Claim(s)]
[Claim 1] The semiconductor chip which a semiconductor circuit element is formed in the principal plane, and has two or more wiring connections on the front face. The tape substrate which consists of an organic system material. Wiring containing two or more inner lead sections connected to two or more lands for external electrodes and aforementioned wiring connections to which it is formed in the aforementioned tape substrate and an outer lead is connected. It is the semiconductor device equipped with the above, and the aforementioned common wiring section and the aforementioned inner lead section are characterized by being what has one or more paths connected directly, without going via the aforementioned land for external electrodes in the aforementioned wiring including the common wiring section connected to at least one land for external electrodes.
[Claim 2] The semiconductor device characterized by being a semiconductor device according to claim 1, forming in the center section of the aforementioned tape substrate opening by which the aforementioned inner lead section is arranged, forming the aforementioned common wiring section along with **** of the aforementioned tape substrate, and forming the aforementioned land for external electrodes between the aforementioned opening and the aforementioned common wiring section.
[Claim 3] The semiconductor device characterized by being a semiconductor device according to claim 1, arranging the aforementioned inner lead section along with **** of the aforementioned tape substrate, forming the aforementioned common wiring section in the center section of the aforementioned tape substrate, and forming the aforementioned land for external electrodes between the aforementioned **** and the aforementioned common wiring section.
[Claim 4] Are a semiconductor device according to claim 1, and the aforementioned tape substrate is divided into the 1st and 2nd tape substrates in the center section of the aforementioned semiconductor chip. The aforementioned common wiring section is formed along the center-section side edge side of each aforementioned semiconductor chip of the above 1st and the 2nd tape substrate. The semiconductor device characterized by forming the aforementioned land for external electrodes in the edge side of each aforementioned semiconductor chip of the above 1st and the 2nd tape substrate, and forming opening by which the aforementioned inner lead section is arranged between the aforementioned common wiring section and the aforementioned land for external electrodes.
[Claim 5] The field in which it is a semiconductor device according to claim 4, and the aforementioned common wiring section of the above 1st and the 2nd tape substrate was formed is a semiconductor device characterized by superimposing mutually and being formed.
[Claim 6] It is the semiconductor device characterized by being a semiconductor device according to claim 1, 2, 3, 4, or 5, and the aforementioned wiring making copper or a copper alloy the main conductive layer.
[Claim 7] It is the manufacture method of a semiconductor device according to claim 1, 2, 3, 4, 5, or 6. (a) The process which forms the conductor thin film which consists of copper or a copper alloy on the aforementioned tape substrate, (b) The process which forms the 1st resist in the field equivalent to the aforementioned wiring and the wiring for electrolysis plating on the aforementioned conductor thin film, (c) The aforementioned conductor thin film is **********ed by using the 1st resist of the above as a mask. All fields **** the process which forms the conductor pattern connected electrically, the process which forms the 2nd resist on the aforementioned wiring for electrolysis plating of the (d) aforementioned conductor pattern, and the (e) aforementioned tape substrate to the electrolytic solution, and energize to a conductor pattern. The process which gold-plates on the front face of the aforementioned conductor pattern except the field covered with the 2nd resist of the above, (f) The manufacture method of the semiconductor device characterized by including the process which removes the 2nd resist of the above, **** the aforementioned tape substrate to the etching reagent which has a selection ratio between copper or a copper alloy, and gold, and removes the aforementioned wiring for electrolysis plating.
[Claim 8] The manufacture method of the semiconductor device characterized by to include the process which is the manufacture method of a semiconductor device according to claim 1, 2, 3, 4, 5, or 6, carries out patterning of the process and the (b) aforementioned conductor thin film which form the conductor thin film which consists of copper or a copper alloy on the (a) aforementioned tape substrate, gives electroless deposition to the process and the (c) aforementioned conductor pattern which form the conductor pattern equivalent to the aforementioned wiring, and forms gold plate in the front face.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[The technical field to which invention belongs] Especially this invention is applied to the area array type surface mount type semiconductor device adapting TCP (Tape Carrier Package) about a semiconductor device, and relates to effective technology.
[0002]
[Description of the Prior Art] In recent years, in semiconductor devices in consideration of application for the use to which the occupancy area of a mounting substrate is restricted remarkably, such as a Personal Digital Assistant or a mobile communications device, the miniaturization of the package is demanded strongly. Moreover, it corresponds to many pin-ization of the semiconductor device having advanced features, and technology of aiming at reduction of the occupancy area to a mounting substrate simultaneously is desired strongly.
[0003] as one of the technology which satisfies such a demand, the technology of TCP which is indicated by November 30, Showa 59, Ohm-Sha Ltd. Issue, and "LSI handbook" p410-p411 is known furthermore, the technology of April 20, Heisei 7, press journal issue, the "monthly Semiconductor World" May, 1995 issue, and CSP (Chip Size Package) that is indicated by p104-p131 is known as technology in which possibility of satisfying the demand of a severe miniaturization or the formation of many pins is high
[0004] Especially, this reference, p112-p113 or May 1, Heisei 6, the Nikkei Business Publications issue, The technology of the "Nikkei micro device" May, 1994 issue and muBGA which is the proposal of U.S. TESERA indicated by p98-p102 It excels in respect of [mounting / flip chip / bare chip mounting or] the plain-gauze fibers for plastering of tests, such as goodness of the standardization ease of a connection pitch, and the absorptivity of the difference in coefficient of thermal expansion, and a burn-in, etc. It excels in respect of [TCP] the ease of handling at the time of mounting etc., and it is thought that it is the technology which was synthetically superior to other mounting technology.
[0005] Although it is indicated in detail by the ****** No. 504408 [six to] official report, the technology of muBGA will be as follows if the outline is explained.
[0006] Namely, the bump as wiring and an outer lead is formed in flexible tapes, such as a polyimide, for example. Consider as the tape substrate of the same area mostly with a semiconductor substrate, and this tape substrate is pasted up on the principal plane of a semiconductor substrate by the glue line which consists of an elastic body. The inner lead of the shape of a gal wing extended and formed from the end face of the through hole which carried out opening to the tape substrate, or a tape substrate is connected to the element electrode of the principal plane of a semiconductor device by heat or ultrasonic sticking by pressure. An inner lead is formed as a part of wiring formed on the tape substrate.
[0007] It is as aforementioned for handling to be easy, while a miniaturization is easy, since the outer lead is formed in the field which corresponds all over a semiconductor substrate with such muBGA technology. Moreover, since between a semiconductor substrate and tape substrates is pasted up by the elastic body, there is an advantage that the relative variation rate between both substrates is possible, and it is possible to ease the thermal stress by the difference of the coefficient of thermal expansion between each part material.
[0008]
[Problem(s) to be Solved by the Invention] However, the above-mentioned technology of muBGA was technology which thought the miniaturization of a semiconductor device, and the ease of handling as important, and has been developed, and was not what was developed in consideration of standardization of a semiconductor device. Therefore, there was fault that the position of the outer lead on a tape substrate will receive restrictions by arrangement of the element electrode on a semiconductor substrate.
[0009] that is, when wiring is formed two-dimensional on a tape substrate, and the technology of muBGA is a tape substrate, while restricts a wiring forming face in consideration of cost, IE, etc. especially like other TCP technology, it is not permitted that between wiring crosses For this reason, as aforementioned, restrictions will arise in the relation between the position of an outer lead, and arrangement of an element electrode, and an outer lead will be assigned in order of arrangement of an element electrode.
[0010] Although such restrictions do not pose a problem so much when the use of a semiconductor device is a custom IC etc., the use of a semiconductor device produces a big problem in general-purpose articles, such as DRAM. That is, in the case of a general-purpose article, the demand which standardizes arrangement of an outer lead will be strong, and it will be the requisite that especially arrangement of a power terminal or an earth terminal is determined beforehand in many cases. In such a case, it is necessary to design the layout of the element electrode on a semiconductor substrate so that arrangement of the outer lead determined beforehand may be suited. Therefore, there is a problem that the flexibility of a design becomes low.
[0011] Moreover, for the improvement in an electrical property of a semiconductor device, it is desirable to prepare many grounding electrodes and power supply electrodes as much as possible. however, an outer lead with the present muBGA technology corresponding to an one to one to an element electrode If improvement in the electrical property of a semiconductor device is meant and many groundings or power terminals are prepared, many number of outer leads will be

formed and are not desirable to the miniaturization of a semiconductor device. On the contrary, when priority was given to the miniaturization of a semiconductor device and the limit was prepared in the number of outer leads, the situation where it became impossible to perform grounding or optimization of a power terminal, and improvement in the performance of a semiconductor device could not fully be aimed at had arisen.
[0012] The purpose of this invention is to offer the technology in which a power terminal and an earth terminal can be prepared on a semiconductor substrate, without receiving restrictions in arrangement of an outer lead.
[0013] Other purposes of this invention are to offer the technology which can standardize outer-lead arrangement of a semiconductor device, without restricting the design flexibility of the element electrode disposition on a semiconductor substrate.
[0014] The purpose of further others of this invention is to offer the technology which can decrease the number of outer leads.
[0015] The purpose of further others of this invention is to offer the technology which can improve the electrical property of a semiconductor device, without increasing the number of outer leads.
[0016] The other purposes and the new feature will become clear from description and the accompanying drawing of this specification at the aforementioned row of this invention.
[0017]
[Means for Solving the Problem] It will be as follows if the outline of a typical thing is briefly explained among invention indicated in this application.
[0018] (1) The semiconductor chip which, as for the semiconductor device of this invention, a semiconductor circuit element is formed in the principal plane, and has two or more wiring connections on the front face, It is the semiconductor device which has wiring containing two or more inner lead sections connected to two or more lands for external electrodes and wiring connections to which it is formed in the tape substrate which consists of an organic system material, and a tape substrate, and an outer lead is connected. The common wiring section and the inner lead section have one or more paths connected directly, without wiring going via the land for external electrodes including the common wiring section which presupposes a part and is connected to at least one land for external electrodes.
[0019] Since the common wiring section and the inner lead section have one or more paths connected directly according to such a semiconductor device, without wiring going via the land for external electrodes including the common wiring section which presupposes a part and is connected to at least one land for external electrodes, a power supply and the element electrode of grounding potential can be arranged on the front face of a semiconductor substrate, without being restricted to arrangement of an outer lead.
[0020] That is, since the land for external electrodes ~~is connected to the common~~ wiring section, the outer lead connected to this land for external electrodes can be used as a power terminal or an earth terminal, and the common wiring section can be ~~held to~~ power supply potential or grounding potential in that case. Furthermore, without going via the land for external electrodes, when the common wiring section and the inner lead section have the path connected directly, the element electrode on the semiconductor substrate connected to this inner lead section can be made into the same potential as the common wiring section, i.e., grounding, and power supply potential. This path can arrange arbitrarily the position of the element electrode which touches the inner lead section by which a direct file is carried out to the common wiring section since between the lands for external electrodes can be sewn and installed, without [that is,] going via the land for external electrodes, without being influenced by arrangement of the land for external electrodes. That is, the arrangement design of an element electrode can be performed arbitrarily, without being restricted to arrangement of the land for external electrodes.
[0021] Consequently, the arrangement design of an element electrode can be made easy to become easy to attain standardization of the outer-lead terminal which is needed when using a semiconductor device as general-purpose articles, such as DRAM, and to perform. Furthermore, since it becomes unnecessary to be able to improve the electrical property of a semiconductor device since the power supply on a semiconductor substrate and the number of grounding electrodes can be increased arbitrarily, and to install many number of outer leads, the number can be decreased to necessary minimum.
[0022] In addition, the relation by which opening and the common wiring section by which the inner lead section is arranged, and the land for external electrodes are arranged may be as follows.
[0023] Namely, opening by which the inner lead section is arranged is formed in the center section of (a) tape substrate. When the common wiring section is formed along with **** of a tape substrate and the land for external electrodes is formed between opening and the common wiring section, (b) The inner lead section is arranged along with **** of a tape substrate, and the common wiring section is formed in the center section of a tape substrate. When the land for external electrodes is formed between **** and the common wiring section, (c) A tape substrate is divided into the 1st and 2nd tape substrates in the center section of the semiconductor chip. The common wiring section is formed along each semiconductor chip center-section side edge side of the 1st and 2nd tape substrates. It is the case where the land for external electrodes is formed in each semiconductor chip edge side of the 1st and 2nd tape substrates, and opening by which the inner lead section is arranged between the common wiring section and the land for external electrodes is formed.
[0024] Furthermore, in the above (c), the field in which the common wiring section of the 1st and 2nd tape substrates was formed can be superimposed mutually, and can be formed. In such a case, it is possible for the occupancy area of the 1st and 2nd tape substrates to become small by the field on which it is superimposed mutually, and to miniaturize a semiconductor device.
[0025] Moreover, wiring of the semiconductor device of this invention should make copper or the copper alloy the main conductive layer, and gold plate should be performed. In such a case, since copper or a copper alloy is used as a main conductive layer compared with the case where all the wiring is manufactured withgold, the cost of a wiring material can be reduced and the manufacturing cost of a semiconductor device can be made low.
[0026] (2) The manufacture method of the semiconductor device of this invention is the manufacture method of the semiconductor device the aforementioned (1) publication. (a) The process which forms the conductor thin film which consists of copper or a copper alloy on a tape substrate, (b) The process which forms the 1st resist in the field equivalent to the wiring and the wiring for electrolysis plating on a conductor thin film, (c) The process which forms the conductor pattern to which the conductor thin film was **********ed by having used the 1st resist as the mask, and all fields were connected

electrically, (d) **** the process and (e) tape substrate which form the 2nd resist on the wiring for electrolysis plating of a conductor pattern to the electrolytic solution, and it energizes to a conductor pattern. The process, and the (f) 2nd resist which gold-plate on the front face of the conductor pattern except the field covered with the 2nd resist are removed, a tape substrate is ****(ed) to the etching reagent which has a selection ratio between copper or a copper alloy, and gold, and the process which removes the wiring for electrolysis plating is included.
[0027] In order to ********** a conductor thin film by using as a mask the 1st resist formed in the field equivalent to wiring and the wiring for electrolysis plating according to the manufacture method of such a semiconductor device, the conductor pattern formed of etching becomes what was connected electrically in all fields, and it has an effect of making easy to perform electrolysis plating which performs henceforth [the following process].
[0028] Moreover, after forming the 2nd resist on the wiring for electrolysis plating, in order to perform electrolysis plating, the 2nd resist serves as a mask, and gold plate is not formed in wiring for electrolysis plating, but it becomes that it is possible in removing the wiring for electrolysis plating easily by the etching processing by ****(ing) to the etching reagent which it has in a selection ratio between the etching processing performed in the following process, i.e., copper, a copper alloy, and gold.
[0029] Thus, this manufacture method enables it to manufacture the semiconductor device of a publication easily to the above (1), without changing like the conventional galvanizer sharply.
[0030] In addition, you may form gold plate in the front face by forming a conductor pattern in the configuration of wiring from the beginning, and giving electroless deposition to a conductor pattern.
[0031] Moreover, although forming with the photolithography technology which used the photoresist is also possible, the screen-stencil technology which can be formed by the low cost more simple may be used for the 1st resist of the above, and the 2nd resist.
[0032]
[Embodiments of the Invention] Hereafter, the gestalt of operation of this invention is explained in detail based on a drawing. In addition, in the complete diagram for explaining the gestalt of operation, the same sign is given to the same member and explanation of the repeat is omitted.
[0033] (Gestalt 1 of operation) Drawing 1 is the perspective diagram having shown an example of the appearance of the semiconductor device which is the gestalt of 1 operation of this invention. In order to make a drawing legible in drawing 1 , the cutting section and a dashed line show some members. Moreover, drawing 2 is III-III [in / drawing 1 and drawing 2 / it is the plan showing the wiring portion of the semiconductor device shown in drawing 1 , and / in drawing 3]. It is a line cross section.
[0034] The semiconductor device of the gestalt 1 of this operation has a semiconductor chip 1 and the tape substrate 2 which consists of an organic system material, a semiconductor circuit element is formed in the principal plane side of a semiconductor chip 1, and the wiring connection 3 is formed as an input/output terminal of the semiconductor circuit element. The wiring connection 3 is arranged in the center section of the semiconductor chip 1, and let them be bumps, such as gold formed on the aluminum pad as a part of wiring layer which is circuit wiring of a semiconductor circuit element, or the pad.
[0035] A polyimide (you PIREKKUSU) can be used for the tape substrate 2, and it can set the thickness to 50 micrometers. It is different from this point and the point of using thickness (75 micrometers or 125 micrometers) of a tape in the usual TCP. Moreover, the tape opening 4 is formed in the center section of the tape substrate 2 corresponding to the array of the wiring connection 3.
[0036] In one field of the tape substrate 2, it has the wiring 5 by which patterning was carried out, and the bump 6 who functions as an outer lead is formed in the field of another side in it.
[0037] Wiring 5 consists of land 5for external electrodes a, inner lead section 5b, common wiring section 5c, and 5d of the lead wiring sections. 28 land 5a for external electrodes is prepared corresponding to 28 outer leads, and 32 inner lead section 5b is prepared corresponding to 32 wiring connections. Two common wiring section 5c is prepared, either is held at grounding potential, and another side is held at power supply potential. 5d of lead wiring sections connects electrically land 5for external electrodes a, inner lead section 5b, and common wiring section 5c mutually.
[0038] the connection whose land 5a for external electrodes carried out opening of the wiring 5 to the tape substrate 2 -- it is a land for connecting with a bump 6 easily through a hole 7, and the thickness can be set to 18 micrometers In addition, you may be a rectangle although it is common to suppose that it is circular as the configuration of land 5a for external electrodes is illustrated. moreover, the path of the bump 6 who explains the path later -- small -- connection -- it is desirable that it is larger than the path of a hole 7, for example, it is 500 micrometers
[0039] Inner lead section 5b is for connecting wiring 5 to the wiring connection 3, and is arranged along with the tape opening 4. That is, form the tape opening 4 so that 32 wiring connections 3 arranged in the center section of the semiconductor chip 1 may be exposed, and extend and form inner lead section 5b arranged by the both sides of the opening from opening ****, it is made to curve at a suitable angle, and an one to one is contacted to the wiring connection 3. Bonding of this contact should be carried out by heat or the ultrasonic wave. In addition, thickness of inner lead section 5b can be set to 18 micrometers, and the width of face can be set to 50 micrometers. Moreover, the interval between inner lead section 5b can be set to 50 micrometers. However, the width of face and interval can be respectively decreased to 25 micrometers.
[0040] Common wiring section 5c is prepared near the both ends of the tape substrate 2, and has a rectangular configuration. The length of the long side is longer than the length of the long side of the tape opening 4 a little. This becomes possible to form the lead wiring directly extended to inner lead section 5b in the arbitrary positions of the direction of the long side of common wiring section 5c. Although the length of the direction of a shorter side of common wiring section 5c, i.e., the width of face of common wiring section 5c, can be made into arbitrary length, it can be set to 50 micrometers equivalent to the width of face of 5d of lead wiring sections, for example. However, since common wiring section 5c uses it as a power supply or grounding wiring so that it may explain later, the width of face is desirable for [, such as noise resistance,] the improvement in an electrical property of a semiconductor device for the method of latus as much as possible. Moreover, thickness of common wiring section 5c can be set to 18 micrometers like other fields of wiring 5. In addition, although

common wiring section 5c was made into the rectangular configuration with the gestalt 1 of this operation, as long as it is longer than the length of the long side of the tape opening 4 a little, the configuration may be arbitrary and may be a rectangle, a wave, a saw form, or a curve.

[0041] Moreover, common wiring section 5c is a part of wiring 5 which is held at grounding potential or power supply potential, and is shared as grounding or power supply wiring. Therefore, common wiring section 5c needs to be connected to at least one of the land 5a for external electrodes equivalent to grounding or a power terminal. In the case of the gestalt 1 of this operation, two common wiring section 5c is prepared, and has grounding common wiring 5c-1 held at grounding potential, and power supply common wiring 5c-2 which are held at power supply potential. Grounding common wiring 5c-1 is connected to grounding external electrode land 5a-1 connected to the bump 6 grounded through grounding lead wiring 5d-1, and four grounding external electrode land 5a-1 are prepared in drawing 2 . Power supply common wiring 5c-2 are connected to power supply external electrode land 5a-2 connected to the power supply bump 6 held through power supply lead wiring 5d-2 at voltage, and two power supply external electrode land 5a-2 are prepared in drawing 2 .

[0042] Furthermore, common wiring section 5c is connectable with direct inner lead section 5b3, i.e., a wiring connection, without land 5a for external electrodes. That is, it is possible to connect with common wiring section 5c with the lead wiring which only arbitrary numbers arrange the wiring connection 3 which becomes a semiconductor chip 1 with grounding or a power terminal in arbitrary positions, and does not such wiring mind [3] inner lead section 5b and land 5a for external electrodes. In the case of the gestalt 1 of this operation, the wiring connection 3 which should be held to grounding potential is connected to grounding common wiring 5c-1 by grounding lead wiring 5d-3 which do not mind inner lead section 5b and land 5a for external electrodes, and the wiring connection 3 which should be held to power supply potential is connected to power supply common wiring 5c-2 by power supply lead wiring 5d-4 which are not minded in inner lead section 5b and land 5a for external electrodes. Such two grounding lead wiring 5d-3 and power supply lead wiring 5d-4 are prepared respectively.

[0043] that to which 5d of lead wiring sections connects respectively land 5for external electrodes a, inner lead section 5b, and common wiring section 5c -- it is -- 5d [of grounding lead wiring] - 1, 3, and 5d [of power supply lead wiring] - 2 and 4 are contained Thickness of 5d of lead wiring sections can be set to 18 micrometers, and the width of face can be set to 50 micrometers. Moreover, the interval can be set to 50 micrometers in the portion which approached most. However, the interval in the width of face and the maximum contiguity section can be respectively decreased to 25 micrometers.

[0044] Wiring 5, i.e., land 5for external electrodes a, inner lead section 5b, common wiring section 5c, and 5d of lead wiring sections have main conductive-layer 5e and 5f of deposits. Main conductive-layer 5e can be made into copper or a copper alloy, and 5f of deposits can be considered as gold plate. Thus, by making main conductive-layer 5e into copper or a copper alloy, sufficient conductivity and sufficient current capacity can be secured, and reduction of cost can be aimed at as compared with the case where gold is made into the main conductive layer. Moreover, by considering 5f of deposits as gold plate, in the manufacturing process of the semiconductor device explained later, in order to remove the copper or the copper alloy portion for electrolysis plating, gold plate can be used as a mask.

[0045] A bump 6 can consider for example, as a solder bump, and can set the path and height of a ball to 600 micrometers and 500 micrometers respectively, for example. However, the path and height can be respectively decreased to 300 micrometers and 200 micrometers.

[0046] the connection in which wiring 5 and the bump 6 did opening to the tape substrate 2 -- it connects through a hole 7 connection -- the diameter of opening of a hole 7 can be reduced to 200 micrometers, although it can be referred to as 450 micrometers

[0047] The semiconductor chip 1 and the tape substrate 2 are pasted up by the glue line 8. Silicone rubber can be illustrated as a material of a glue line 8. While a glue line 8 acts as adhesives of a semiconductor chip 1 and the tape substrate 2, it can act also as an elastic body and can set the elastic modulus to 0.1-50MPa. By making a glue line 8 into an elastic body, the thermal stress by difference of a coefficient of thermal expansion can be absorbed, and the reliability of mounting of a semiconductor device can be improved.

[0048] The tape opening 4 is closed by resin 9. By embedding resin 9, inner lead section 5b and a semiconductor chip 1 can be protected.

[0049] According to the semiconductor device of the gestalt 1 of this operation, since common wiring section 5c is prepared, the wiring connection 3 held at grounding and supply voltage of numbers arbitrary on a semiconductor chip 1 and arrangement can be formed. That is, the wiring connection 3 of the grounding voltage arranged arbitrarily can be connected to grounding common wiring 5c-1 through land 5a for external electrodes through grounding lead wiring 5d-3, and, in such a case, arrangement of the wiring connection 3 of the grounding voltage arranged arbitrarily does not influence arrangement of the bump 6 who is an outer lead. Moreover, the wiring connection 3 of the supply voltage arranged arbitrarily can be connected to power supply common wiring 5c-2 through land 5a for external electrodes through power supply lead wiring 5d-4, and arrangement of the wiring connection 3 of the supply voltage which has been arranged arbitrarily also in such a case does not influence arrangement of the bump 6 who is an outer lead. Consequently, irrespective of arrangement of an outer lead, the arrangement design of the wiring connection 3 can be performed and the design flexibility can be responded also to standardization of increase and a semiconductor device. Moreover, since arbitrary numbers of power supplies and earth terminals can be prepared in the wiring connection 3, the number of outer leads can be decreased and the electrical property of semiconductor devices, such as noise figure, can be improved.

[0050] Next, the manufacture method of the semiconductor device of the gestalt 1 this operation is explained using drawing 4 - drawing 11 . Drawing 4 - drawing 9 show an example of the manufacture method of the semiconductor device of the gestalt 1 of operation in order of the process, (a) is a bottom plan view and (b) is a b-b line cross section in (a). Moreover, drawing 10 and drawing 11 are the cross sections having shown an example of the manufacture method of the semiconductor device of the gestalt 1 of operation in order of the process.

[0051] First, the thin film 11 of copper of about 18 micrometers of thickness or a copper alloy is formed in one side of the polyimide tape 10 which has the thickness of 50 micrometers (drawing 4).

[0052] Next, a resist is formed in both sides of the thin film 11 of copper or a copper alloy, and the thin film 11 of copper or a copper alloy is **********ed to them by using this resist as a mask. Patterning of this resist is carried out to the pattern

equivalent to the wiring 5 and the wiring 12 for gold plate which are formed behind, and main conductive-layer 5e of wiring 5 and the wiring 12 for gold plate are formed as a result of patterning (drawing 5). In addition, in order to make a drawing legible in drawing 5 , main conductive-layer 5e of wiring 5 is a solid line, and a dashed line shows the wiring 12 for gold plate. Moreover, formation of a resist can use well-known screen printing or photolithography technology, and etching can use the well-known wet etching method or the dry etching method.

[0053] Next, a resist 13 is formed so that the wiring 12 for gold plate may be covered (drawing 6). Formation of a resist can use well-known screen printing or photolithography technology. Then, the polyimide tape 10 is ****(ed) to the electrolytic solution, it energizes to the wiring 12 for gold plate, and main conductive-layer 5e, and 5f of deposits which consist of gold plate is formed in the field, i.e., the front face of main conductive-layer 5e, with which the resist 13 is not covered (drawing 6 (c)).

[0054] Next, a resist 13 is removed (drawing 7). If it does so, it will expose in the state [that the portion of the wiring 12 for gold plate with which gold plate is not formed continues being copper or a copper alloy].

[0055] The polyimide tape 10 which such copper or a copper alloy exposed is ****(ed) to an etching reagent, the wiring 12 for gold plate is removed, and wiring 5 is formed (drawing 8). Mixed-acid liquid, such as liquid with which copper or a copper alloy **********s and gold does not **********, for example, a nitric acid, and an acetic acid, can be used for an etching reagent.

[0056] next, the polyimide tape 10 -- connection -- a hole 7 and the tape opening 4 are formed (drawing 9) Under the present circumstances, inner lead section 5b is formed. The ablation method by laser can be used for removal of the polyimide tape 10.

[0057] next, connection -- the bump 6 who becomes the portion of a hole 7 from solder is formed (drawing 9 (c)) A bump 6 can form for example, by electrolysis plating. The tape substrate 2 can be formed as mentioned above.

[0058] Next, the tape substrate 2 is pasted up on a semiconductor chip 1 through a glue line 8 (drawing 10). The silicone system resin is suitable as aforementioned, and a glue line 8 is effective in raising the connection reliability of an outer lead. In addition, thickness of a glue line 8 can be set to 150 micrometers.

[0059] Next, it pushes to the wiring connection 3, making a tool 14 act on the lead edge of inner lead section 5b, and bending inner lead section 5b. Furthermore, ultrasonic energy is impressed to a tool 14 and the edge and the wiring connection 3 of inner lead section 5b are connected to it (drawing 11). As a method of connection, gang bonding (package method) well-known as the bonding method of TCP or single point bonding can be used. In addition, in addition to ultrasonic energy, you may use the bonding by heating together.

[0060] Finally, the tape opening 4 is filled up with resin 9, and the semiconductor device shown in drawing 1 - drawing 3 is completed.

[0061] Since according to the manufacture method of the semiconductor device of the gestalt this operation it becomes easy to impress the current for electrolysis plating, and the wiring 12 for gold plate is covered by the resist 13 and electrolysis plating is performed in order to connect all main conductive-layer 5e of wiring 5 with the wiring 12 for gold plate and to consider as one pattern, it becomes that it is possible to gold-plate only on the front face of main conductive-layer 5e. Consequently, in the etching process at the time of **********ing the wiring 12 for gold plate and forming wiring 5, 5f of deposits can be used as a mask, and it becomes possible to perform the formation process of wiring 5 simple.

[0062] In addition, without forming the wiring 12 for gold plate in the above-mentioned manufacture method, the pattern of main conductive-layer 5e which is equivalent to the pattern of wiring 5 at once is formed, after that, 5f of deposits which consist of gold plate by electroless deposition may be formed, and wiring 5 may be formed.

[0063] (Gestalt 2 of operation) Drawing 12 is the plan showing the wiring portion of the semiconductor device which is the gestalt of other operations of this invention, and drawing 13 is a XIII-XIII line cross section in drawing 12 .

[0064] The wiring connection 3 by which the semiconductor device of the gestalt 2 of this operation was formed on the semiconductor chip 1 is arranged to the edge field of a semiconductor chip 1, and inner lead section 5b therefore connected to the wiring connection 3 is also arranged by **** of the tape substrate 2 corresponding to it. In such a case, common wiring section 5c can be arranged in the center section of the tape substrate 2, and it can be connected to inner lead section 5b which corresponds directly, without going via land 5a for external electrodes in the wiring connection 3 which should be held from common wiring section 5c to grounding potential or power supply potential. Therefore, the same effect as the gestalt 1 of operation can be acquired. Common wiring section 5c may be not only the shape of a rectangle but a rectangle, a wave, a saw form, or a curve.

[0065] in addition, land 5for external electrodes a, 5d of lead wiring sections, a bump 6, and connection -- since the hole 7, the glue line 8, and the resin 9 grade are the same as that of the gestalt 1 of operation, explanation is omitted Suppose that the manufacture method is the same as that of the gestalt 1 of operation. In addition, in the case of the gestalt 2 of this operation, tape opening is not prepared.

[0066] (Gestalt 3 of operation) Drawing 14 is the plan showing the wiring portion of the semiconductor device of this invention which is the gestalt of other operations further, and drawing 15 is a XV-XV line cross section in drawing 14 .

[0067] As for the semiconductor device of the gestalt 3 of this operation, it has two tape substrates 2 by cutting the tape substrate 2 in the center section of the semiconductor chip 1, and the tape opening 4 is formed in the semiconductor chip 1 central approach of each tape substrate 2. Common wiring section 5c is installed along the semiconductor chip 1 center-section side edge side of each tape substrate 2, and land 5a for external electrodes is arranged on the semiconductor chip 1 outside of each tape substrate 2.

[0068] Also in such a case, it can connect with inner lead section 5b which corresponds directly, without going via land 5a for external electrodes in the wiring connection 3 which should be held from common wiring section 5c to grounding potential or power supply potential, and the same effect as the gestalt 1 of operation can be acquired. The configuration of common wiring section 5c may also be a rectangle which was stated with the gestalten 1 and 2 of the aforementioned implementation, a wave, a saw form, or a curve.

[0069] in addition, 5d of lead wiring sections, a bump 6, and connection -- since the hole 7, the glue line 8, and the resin 9 grade are the same as that of the gestalt 1 of operation, explanation is omitted Suppose that the manufacture method is the same as that of the gestalt 1 of operation.

[0070] Moreover, when it has the tape substrate 2 divided into two like the gestalt 3 of this operation, as shown in drawing 16 and drawing 17 , it is possible to form the field of common wiring section 5c of the tape substrate 2 in piles. Drawing 16 is the plan showing the wiring portion of other examples of the semiconductor device of this invention which is the gestalt of other operations further, and drawing 17 is a XVII-XVII line cross section in drawing 16 . In such a case, in order to form common wiring section 5c of the tape substrate 2 in piles, it becomes possible to reduce the area occupied by the tape substrate 2 whole, and it becomes possible to attain the miniaturization of a semiconductor device.
[0071] As mentioned above, although invention made by this invention person was concretely explained based on the gestalt of implementation of invention, it cannot be overemphasized by this invention that it can change variously in the range which is not limited to the gestalt of the aforementioned implementation and does not deviate from the summary.
[0072] For example, although you may be other organic system material although the case of a polyimide was illustrated for the tape substrate 2 with the gestalt of this operation, and a bump's 6 quality of the material was used as solder, it cannot be overemphasized that you may be a golden bump.
[0073]
[Effect of the Invention] It will be as follows if the effect acquired by the typical thing among invention indicated in this application is explained briefly.
[0074] (1) A power terminal and an earth terminal can be prepared on a semiconductor substrate, without receiving restrictions in arrangement of an outer lead.
[0075] (2) Outer-lead arrangement of a semiconductor device can be standardized, without restricting the design flexibility of the element electrode disposition on a semiconductor substrate.
[0076] (3) The number of outer leads can be decreased.
[0077] (4) The electrical property of a semiconductor device can be improved, without increasing the number of outer leads.

[Translation done.]

* NOTICES *

1. This document has been translated by computer.So the translation may not reflect the original precisely.
2. **** shows the word which can not be translated.
3.In the drawings, any words are not translated.

TECHNICAL FIELD

[The technical field to which invention belongs] Especially this invention is applied to the area array type surface mount type semiconductor device adapting TCP (Tape Carrier Package) about a semiconductor device, and relates to effective technology.

[Translation done.]

PRIOR ART

[Description of the Prior Art] In recent years, in semiconductor devices in consideration of application for the use to which the occupancy area of a mounting substrate is restricted remarkably, such as a Personal Digital Assistant or a mobile communications device, the miniaturization of the package is demanded strongly. Moreover, it corresponds to many pin-ization of the semiconductor device having advanced features, and technology of aiming at reduction of the occupancy area to a mounting substrate simultaneously is desired strongly.

[0003] as one of the technology which satisfies such a demand, the technology of TCP which is indicated by November 30, Showa 59, Ohm-Sha Ltd. Issue, and "LSI handbook" p410-p411 is known furthermore, the technology of April 20, Heisei 7, press journal issue, the "monthly Semiconductor World" May, 1995 issue, and CSP (Chip Size Package) that is indicated by p104-p131 is known as technology in which possibility of satisfying the demand of a severe miniaturization or the formation of many pins is high

[0004] Especially, this reference, p112-p113 or May 1, Heisei 6, the Nikkei Business Publications issue, The technology of the "Nikkei micro device" May, 1994 issue and muBGA which is the proposal of U.S. TESERA indicated by p98-p102 It excels in respect of [mounting / flip chip / bare chip mounting or] the plain-gauze fibers for plastering of tests, such as goodness of the standardization ease of a connection pitch, and the absorptivity of the difference in coefficient of thermal expansion, and a burn-in, etc., and excels in respect of / TCP / the ease of handling at the time of mounting etc. It is thought that it is the technology which was synthetically superior to other mounting technology.

[0005] Although it is indicated in detail by the ****** No. 504408 [six to] official report, the technology of muBGA will be as follows if the outline is explained.

[0006] Namely, glue lines which form the bump as wiring and an outer lead in a flexible tape, consider as the tape substrate of the same area mostly with a semiconductor substrate, and consist this tape substrate of an elastic body, such as a polyimide. The principal plane of a semiconductor substrate is pasted and the inner lead of the shape of a gal wing extended and formed from the end face of the through hole which carried out opening to the tape substrate, or a tape substrate is connected to the element electrode of the principal plane of a semiconductor device by heat or ultrasonic sticking by pressure. An inner lead is formed as a part of wiring formed on the tape substrate.

[0007] It is as aforementioned for handling to be easy, while a miniaturization is easy, since the outer lead is formed in the field which corresponds all over a semiconductor substrate with such muBGA technology. Moreover, since between a semiconductor substrate and tape substrates is pasted up by the elastic body, there is an advantage that the relative variation rate between both substrates is possible, and it is possible to ease the thermal stress by the difference of the coefficient of thermal expansion between each part material.

[Translation done.]

EFFECT OF THE INVENTION

[Effect of the Invention] It will be as follows if the effect acquired by the typical thing among invention indicated in this application is explained briefly.
[0074] (1) A power terminal and an earth terminal can be prepared on a semiconductor substrate, without receiving restrictions in arrangement of an outer lead.
[0075] (2) Outer-lead arrangement of a semiconductor device can be standardized, without restricting the design flexibility of the element electrode disposition on a semiconductor substrate.
[0076] (3) The number of outer leads can be decreased.
[0077] (4) The electrical property of a semiconductor device can be improved, without increasing the number of outer leads.

[Translation done.]

TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] However, the above-mentioned technology of muBGA was technology which thought the miniaturization of a semiconductor device, and the ease of handling as important, and has been developed, and was not what was developed in consideration of standardization of a semiconductor device. Therefore, there was fault that the position of the outer lead on a tape substrate will receive restrictions by arrangement of the element electrode on a semiconductor substrate.

[0009] that is, when wiring is formed two-dimensional on a tape substrate, and the technology of muBGA is a tape substrate, while restricts a wiring forming face in consideration of cost, IE, etc. especially like other TCP technology, it is not permitted that between wiring crosses For this reason, as aforementioned, restrictions will arise in the relation between the position of an outer lead, and arrangement of an element electrode, and an outer lead will be assigned in order of arrangement of an element electrode.

[0010] Although such restrictions do not pose a problem so much when the use of a semiconductor device is a custom IC etc., the use of a semiconductor device produces a big problem in general-purpose articles, such as DRAM. That is, in the case of a general-purpose article, the demand which standardizes arrangement of an outer lead will be strong, and it will be the requisite that especially arrangement of a power terminal or an earth terminal is determined beforehand in many cases. In such a case, it is necessary to design the layout of the element electrode on a semiconductor substrate so that arrangement of the outer lead determined beforehand may be suited. Therefore, there is a problem that the flexibility of a design becomes low.

[0011] Moreover, for the improvement in an electrical property of a semiconductor device, it is desirable to prepare many grounding electrodes and power supply electrodes as much as possible. however, an outer lead with the present muBGA technology corresponding to an one to one to an element electrode If improvement in the electrical property of a semiconductor device is meant and many groundings or power terminals are prepared, many number of outer leads will be formed and are not desirable to the miniaturization of a semiconductor device. On the contrary, when priority was given to the miniaturization of a semiconductor device and the limit was prepared in the number of outer leads, the situation where it became impossible to perform grounding or optimization of a power terminal, and improvement in the performance of a semiconductor device could not fully be aimed at had arisen.

[0012] The purpose of this invention is to offer the technology in which a power terminal and an earth terminal can be prepared on a semiconductor substrate, without receiving restrictions in arrangement of an outer lead.

[0013] Other purposes of this invention are to offer the technology which can standardize outer-lead arrangement of a semiconductor device, without restricting the design flexibility of the element electrode disposition on a semiconductor substrate.

[0014] The purpose of further others of this invention is to offer the technology which can decrease the number of outer leads.

[0015] The purpose of further others of this invention is to offer the technology which can improve the electrical property of a semiconductor device, without increasing the number of outer leads.

[0016] The other purposes and the new feature will become clear from description and the accompanying drawing of this specification at the aforementioned row of this invention.

[Translation done.]

MEANS

[Means for Solving the Problem] It will be as follows if the outline of a typical thing is briefly explained among invention indicated in this application.
[0018] (1) The semiconductor chip which, as for the semiconductor device of this invention, a semiconductor circuit element is formed in the principal plane, and has two or more wiring connections on the front face, It is the semiconductor device which has wiring containing two or more inner lead sections connected to two or more lands for external electrodes and wiring connections to which it is formed in the tape substrate which consists of an organic system material, and a tape substrate, and an outer lead is connected. The common wiring section and the inner lead section have one or more paths connected directly, without wiring going via the land for external electrodes including the common wiring section which presupposes a part and is connected to at least one land for external electrodes.
[0019] Since the common wiring section and the inner lead section have one or more paths connected directly according to such a semiconductor device, without wiring going via the land for external electrodes including the common wiring section which presupposes a part and is connected to at least one land for external electrodes, a power supply and the element electrode of grounding potential can be arranged on the front face of a semiconductor substrate, without being restricted to arrangement of an outer lead.
[0020] That is, since the land for external electrodes is connected to the common wiring section, the outer lead connected to this land for external electrodes can be used as a power terminal or an earth terminal, and the common wiring section can be held to power supply potential or grounding potential in that case. Furthermore, without going via the land for external electrodes, when the common wiring section and the inner lead section have the path connected directly, the element electrode on the semiconductor substrate connected to this inner lead section can be made into the same potential as the common wiring section, i.e., grounding, and power supply potential. This path can arrange arbitrarily the position of the element electrode which touches the inner lead section by which a direct file is carried out to the common wiring section since between the lands for external electrodes can be sewn and installed, without [that is,] going via the land for external electrodes, without being influenced by arrangement of the land for external electrodes. That is, the arrangement design of an element electrode can be performed arbitrarily, without being restricted to arrangement of the land for external electrodes.
[0021] Consequently, the arrangement design of an element electrode can be made easy to become easy to attain standardization of the outer-lead terminal which is needed when using a semiconductor device as general-purpose articles, such as DRAM, and to perform. Furthermore, since it becomes unnecessary to be able to improve the electrical property of a semiconductor device since the power supply on a semiconductor substrate and the number of grounding electrodes can be increased arbitrarily, and to install many number of outer leads, the number can be decreased to necessary minimum.
[0022] In addition, the relation by which opening and the common wiring section by which the inner lead section is arranged, and the land for external electrodes are arranged may be as follows.
[0023] Namely, opening by which the inner lead section is arranged is formed in the center section of (a) tape substrate. When the common wiring section is formed along with **** of a tape substrate and the land for external electrodes is formed between opening and the common wiring section, (b) The inner lead section is arranged along with **** of a tape substrate, and the common wiring section is formed in the center section of a tape substrate. When the land for external electrodes is formed between **** and the common wiring section, (c) A tape substrate is divided into the 1st and 2nd tape substrates in the center section of the semiconductor chip. The common wiring section is formed along each semiconductor chip center-section side edge side of the 1st and 2nd tape substrates. It is the case where the land for external electrodes is formed in each semiconductor chip edge side of the 1st and 2nd tape substrates, and opening by which the inner lead section is arranged between the common wiring section and the land for external electrodes is formed.
[0024] Furthermore, in the above (c), the field in which the common wiring section of the 1st and 2nd tape substrates was formed can be superimposed mutually, and can be formed. In such a case, it is possible for the occupancy area of the 1st and 2nd tape substrates to become small by the field on which it is superimposed mutually, and to miniaturize a semiconductor device.
[0025] Moreover, wiring of the semiconductor device of this invention should make copper or the copper alloy the main conductive layer, and gold plate should be performed. In such a case, since copper or a copper alloy is used as a main conductive layer compared with the case where all the wiring is manufactured withgold, the cost of a wiring material can be reduced and the manufacturing cost of a semiconductor device can be made low.
[0026] (2) The manufacture method of the semiconductor device of this invention is the manufacture method of the semiconductor device the aforementioned (1) publication. (a) The process which forms the conductor thin film which consists of copper or a copper alloy on a tape substrate, (b) The process which forms the 1st resist in the field equivalent to the wiring and the wiring for electrolysis plating on a conductor thin film, (c) The process which forms the conductor pattern to which the conductor thin film was **********ed by having used the 1st resist as the mask, and all fields were connected electrically, (d) **** the process and (e) tape substrate which form the 2nd resist on the wiring for electrolysis plating of a conductor pattern to the electrolytic solution, and it energizes to a conductor pattern. The process, and the (f) 2nd resist which gold-plate on the front face of the conductor pattern except the field covered with the 2nd resist are removed, a tape substrate is ****(ed) to the etching reagent which has a selection ratio between copper or a copper alloy, and gold, and the

process which removes the wiring for electrolysis plating is included.
[0027] In order to ********** a conductor thin film by using as a mask the 1st resist formed in the field equivalent to wiring and the wiring for electrolysis plating according to the manufacture method of such a semiconductor device, the conductor pattern formed of etching becomes what was connected electrically in all fields, and it has an effect of making easy to perform electrolysis plating which performs henceforth [the following process].
[0028] Moreover, after forming the 2nd resist on the wiring for electrolysis plating, in order to perform electrolysis plating, the 2nd resist serves as a mask, and gold plate is not formed in wiring for electrolysis plating, but it becomes that it is possible in removing the wiring for electrolysis plating easily by the etching processing by ****(ing) to the etching reagent which it has in a selection ratio between the etching processing performed in the following process, i.e., copper, a copper alloy, and gold.
[0029] Thus, this manufacture method enables it to manufacture the semiconductor device of a publication easily to the above (1), without changing like the conventional galvanizer sharply.
[0030] In addition, you may form gold plate in the front face by forming a conductor pattern in the configuration of wiring from the beginning, and giving electroless deposition to a conductor pattern.
[0031] Moreover, although forming with the photolithography technology which used the photoresist is also possible, the screen-stencil technology which can be formed by the low cost more simple may be used for the 1st resist of the above, and the 2nd resist.
[0032]
[Embodiments of the Invention] Hereafter, the gestalt of operation of this invention is explained in detail based on a drawing. In addition, in the complete diagram for explaining the gestalt of operation, the same sign is given to the same member and explanation of the repeat is omitted.
[0033] (Gestalt 1 of operation) Drawing 1 is the perspective diagram having shown an example of the appearance of the semiconductor device which is the gestalt of 1 operation of this invention. In order to make a drawing legible in drawing 1 , the cutting section and a dashed line show some members. Moreover, drawing 2 is III-III [in / drawing 1 and drawing 2 / it is the plan showing the wiring portion of the semiconductor device shown in drawing 1 , and / in drawing 3]. It is a line cross section.
[0034] The semiconductor device of the gestalt 1 of this operation has a semiconductor chip 1 and the tape substrate 2 which consists of an organic system material, a semiconductor circuit element is formed in the principal plane side of a semiconductor chip 1, and the wiring connection 3 is formed as an input/output terminal of the semiconductor circuit element. The wiring connection 3 is arranged in the center section of the semiconductor chip 1, and let them be bumps, such as gold formed on the aluminum pad as a part of wiring layer which is circuit wiring of a semiconductor circuit element, or the pad.
[0035] A polyimide (you PIREKKUSU) can be used for the tape substrate 2, and it can set the thickness to 50 micrometers. It is different from this point and the point of using thickness (75 micrometers or 125 micrometers) of a tape in the usual TCP. Moreover, the tape opening 4 is formed in the center section of the tape substrate 2 corresponding to the array of the wiring connection 3.
[0036] In one field of the tape substrate 2, it has the wiring 5 by which patterning was carried out, and the bump 6 who functions as an outer lead is formed in the field of another side in it.
[0037] Wiring 5 consists of land 5for external electrodes a, inner lead section 5b, common wiring section 5c, and 5d of the lead wiring sections. 28 land 5a for external electrodes is prepared corresponding to 28 outer leads, and 32 inner lead section 5b is prepared corresponding to 32 wiring connections. Two common wiring section 5c is prepared, either is held at grounding potential, and another side is held at power supply potential. 5d of lead wiring sections connects electrically land 5for external electrodes a, inner lead section 5b, and common wiring section 5c mutually.
[0038] the connection whose land 5a for external electrodes carried out opening of the wiring 5 to the tape substrate 2 -- it is a land for connecting with a bump 6 easily through a hole 7, and the thickness can be set to 18 micrometers In addition, you may be a rectangle although it is common to suppose that it is circular as the configuration of land 5a for external electrodes is illustrated. moreover, the path of the bump 6 who explains the path later -- small -- connection -- it is desirable that it is larger than the path of a hole 7, for example, it is 500 micrometers
[0039] Inner lead section 5b is for connecting wiring 5 to the wiring connection 3, and is arranged along with the tape opening 4. That is, form the tape opening 4 so that 32 wiring connections 3 arranged in the center section of the semiconductor chip 1 may be exposed, and extend and form inner lead section 5b arranged by the both sides of the opening from opening ****, it is made to curve at a suitable angle, and an one to one is contacted to the wiring connection 3. Bonding of this contact should be carried out by heat or the ultrasonic wave. In addition, thickness of inner lead section 5b can be set to 18 micrometers, and the width of face can be set to 50 micrometers. Moreover, the interval between inner lead section 5b can be set to 50 micrometers. However, the width of face and interval can be respectively decreased to 25 micrometers.
[0040] Common wiring section 5c is prepared near the both ends of the tape substrate 2, and has a rectangular configuration. The length of the long side is longer than the length of the long side of the tape opening 4 a little. This becomes possible to form the lead wiring directly extended to inner lead section 5b in the arbitrary positions of the direction of the long side of common wiring section 5c. Although the length of the direction of a shorter side of common wiring section 5c, i.e., the width of face of common wiring section 5c, can be made into arbitrary length, it can be set to 50 micrometers equivalent to the width of face of 5d of lead wiring sections, for example. However, since common wiring section 5c uses it as a power supply or grounding wiring so that it may explain later, the width of face is desirable for [, such as noise resistance,] the improvement in an electrical property of a semiconductor device for the method of latus as much as possible. Moreover, thickness of common wiring section 5c can be set to 18 micrometers like other fields of wiring 5. In addition, although common wiring section 5c was made into the rectangular configuration with the gestalt 1 of this operation, as long as it is longer than the length of the long side of the tape opening 4 a little, the configuration may be arbitrary and may be a rectangle, a wave, a saw form, or a curve.
[0041] Moreover, common wiring section 5c is a part of wiring 5 which is held at grounding potential or power supply

potential, and is shared as grounding or power supply wiring. Therefore, common wiring section 5c needs to be connected to at least one of the land 5a for external electrodes equivalent to grounding or a power terminal. In the case of the gestalt 1 of this operation, two common wiring section 5c is prepared, and has grounding common wiring 5c-1 held at grounding potential, and power supply common wiring 5c-2 which are held at power supply potential. Grounding common wiring 5c-1 is connected to grounding external electrode land 5a-1 connected to the bump 6 grounded through grounding lead wiring 5d-1, and four grounding external electrode land 5a-1 are prepared in drawing 2 . Power supply common wiring 5c-2 are connected to power supply external electrode land 5a-2 connected to the power supply bump 6 held through power supply lead wiring 5d-2 at voltage, and two power supply external electrode land 5a-2 are prepared in drawing 2 .

[0042] Furthermore, common wiring section 5c is connectable with direct inner lead section 5b3, i.e., a wiring connection, without land 5a for external electrodes. That is, it is possible to connect with common wiring section 5c with the lead wiring which only arbitrary numbers arrange the wiring connection 3 which becomes a semiconductor chip 1 with grounding or a power terminal in arbitrary positions, and does not such wiring mind [3] inner lead section 5b and land 5a for external electrodes. In the case of the gestalt 1 of this operation, the wiring connection 3 which should be held to grounding potential is connected to grounding common wiring 5c-1 by grounding lead wiring 5d-3 which do not mind inner lead section 5b and land 5a for external electrodes, and the wiring connection 3 which should be held to power supply potential is connected to power supply common wiring 5c-2 by power supply lead wiring 5d-4 which are not minded in inner lead section 5b and land 5a for external electrodes. Such two grounding lead wiring 5d-3 and power supply lead wiring 5d-4 are prepared respectively.

[0043] that to which 5d of lead wiring sections connects respectively land 5for external electrodes a, inner lead section 5b, and common wiring section 5c -- it is -- 5d [of grounding lead wiring] - 1, 3, and 5d [of power supply lead wiring] - 2 and 4 are contained Thickness of 5d of lead wiring sections can be set to 18 micrometers, and the width of face can be set to 50 micrometers. Moreover, the interval can be set to 50 micrometers in the portion which approached most. However, the interval in the width of face and the maximum contiguity section can be respectively decreased to 25 micrometers.

[0044] Wiring 5, i.e., land 5for external electrodes a, inner lead section 5b, common wiring section 5c, and 5d of lead wiring sections have main conductive-layer 5e and 5f of deposits. Main conductive-layer 5e can be made into copper or a copper alloy, and 5f of deposits can be considered as gold plate. Thus, by making main conductive-layer 5e into copper or a copper alloy, sufficient conductivity and sufficient current capacity can be secured, and reduction of cost can be aimed at as compared with the case where gold is made into the main conductive layer. Moreover, by considering 5f of deposits as gold plate, in the manufacturing process of the semiconductor device explained later, in order to remove the copper or the copper alloy portion for electrolysis plating, gold plate can be used as a mask.

[0045] A bump 6 can consider for example, as a solder bump, and can set the path and height of a ball to 600 micrometers and 500 micrometers respectively, for example. However, the path and height can be respectively decreased to 300 micrometers and 200 micrometers.

[0046] the connection in which wiring 5 and the bump 6 did opening to the tape substrate 2 -- it connects through a hole 7 connection -- the diameter of opening of a hole 7 can be reduced to 200 micrometers, although it can be referred to as 450 micrometers

[0047] The semiconductor chip 1 and the tape substrate 2 are pasted up by the glue line 8. Silicone rubber can be illustrated as a material of a glue line 8. While a glue line 8 acts as adhesives of a semiconductor chip 1 and the tape substrate 2, it can act also as an elastic body and can set the elastic modulus to 0.1-50MPa. By making a glue line 8 into an elastic body, the thermal stress by difference of a coefficient of thermal expansion can be absorbed, and the reliability of mounting of a semiconductor device can be improved.

[0048] The tape opening 4 is closed by resin 9. By embedding resin 9, inner lead section 5b and a semiconductor chip 1 can be protected.

[0049] According to the semiconductor device of the gestalt 1 of this operation, since common wiring section 5c is prepared, the wiring connection 3 held at grounding and supply voltage of numbers arbitrary on a semiconductor chip 1 and arrangement can be formed. That is, the wiring connection 3 of the grounding voltage arranged arbitrarily can be connected to grounding common wiring 5c-1 through land 5a for external electrodes through grounding lead wiring 5d-3, and, in such a case, arrangement of the wiring connection 3 of the grounding voltage arranged arbitrarily does not influence arrangement of the bump 6 who is an outer lead. Moreover, the wiring connection 3 of the supply voltage arranged arbitrarily can be connected to power supply common wiring 5c-2 through land 5a for external electrodes through power supply lead wiring 5d-4, and arrangement of the wiring connection 3 of the supply voltage which has been arranged arbitrarily also in such a case does not influence arrangement of the bump 6 who is an outer lead. Consequently, irrespective of arrangement of an outer lead, the arrangement design of the wiring connection 3 can be performed and the design flexibility can be responded also to standardization of increase and a semiconductor device. Moreover, since arbitrary numbers of power supplies and earth terminals can be prepared in the wiring connection 3, the number of outer leads can be decreased and the electrical property of semiconductor devices, such as noise figure, can be improved.

[0050] Next, the manufacture method of the semiconductor device of the gestalt 1 this operation is explained using drawing 4 - drawing 11 . Drawing 4 - drawing 9 show an example of the manufacture method of the semiconductor device of the gestalt 1 of operation in order of the process, (a) is a bottom plan view and (b) is a b-b line cross section in (a). Moreover, drawing 10 and drawing 11 are the cross sections having shown an example of the manufacture method of the semiconductor device of the gestalt 1 of operation in order of the process.

[0051] First, the thin film 11 of copper of about 18 micrometers of thickness or a copper alloy is formed in one side of the polyimide tape 10 which has the thickness of 50 micrometers (drawing 4).

[0052] Next, a resist is formed in both sides of the thin film 11 of copper or a copper alloy, and the thin film 11 of copper or a copper alloy is **********ed to them by using this resist as a mask. Patterning of this resist is carried out to the pattern equivalent to the wiring 5 and the wiring 12 for gold plate which are formed behind, and main conductive-layer 5e of wiring 5 and the wiring 12 for gold plate are formed as a result of patterning (drawing 5). In addition, in order to make a drawing legible in drawing 5 , main conductive-layer 5e of wiring 5 is a solid line, and a dashed line shows the wiring 12 for gold plate. Moreover, formation of a resist can use well-known screen printing or photolithography technology, and etching can

use the well-known wet etching method or the dry etching method.
[0053] Next, a resist 13 is formed so that the wiring 12 for gold plate may be covered (drawing 6). Formation of a resist can use well-known screen printing or photolithography technology. Then, the polyimide tape 10 is ****(ed) to the electrolytic solution, it energizes to the wiring 12 for gold plate, and main conductive-layer 5e, and 5f of deposits which consist of gold plate is formed in the field, i.e., the front face of main conductive-layer 5e, with which the resist 13 is not covered (drawing 6 (c)).
[0054] Next, a resist 13 is removed (drawing 7). If it does so, it will expose in the state [that the portion of the wiring 12 for gold plate with which gold plate is not formed continues being copper or a copper alloy].
[0055] The polyimide tape 10 which such copper or a copper alloy exposed is ****(ed) to an etching reagent, the wiring 12 for gold plate is removed, and wiring 5 is formed (drawing 8). Mixed-acid liquid, such as liquid with which copper or a copper alloy **********s and gold does not **********, for example, a nitric acid, and an acetic acid, can be used for an etching reagent.
[0056] next, the polyimide tape 10 -- connection -- a hole 7 and the tape opening 4 are formed (drawing 9) Under the present circumstances, inner lead section 5b is formed. The ablation method by laser can be used for removal of the polyimide tape 10.
[0057] next, connection -- the bump 6 who becomes the portion of a hole 7 from solder is formed (drawing 9 (c)) A bump 6 can form for example, by electrolysis plating. The tape substrate 2 can be formed as mentioned above.
[0058] Next, the tape substrate 2 is pasted up on a semiconductor chip 1 through a glue line 8 (drawing 10). The silicone system resin is suitable as aforementioned, and a glue line 8 is effective in raising the connection reliability of an outer lead. In addition, thickness of a glue line 8 can be set to 150 micrometers.
[0059] Next, it pushes to the wiring connection 3, making a tool 14 act on the lead edge of inner lead section 5b, and bending inner lead section 5b. Furthermore, ultrasonic energy is impressed to a tool 14 and the edge and the wiring connection 3 of inner lead section 5b are connected to it (drawing 11). As a method of connection, gang bonding (package method) well-known as the bonding method of TCP or single point bonding can be used. In addition, in addition to ultrasonic energy, you may use the bonding by heating together.
[0060] Finally, the tape opening 4 is filled up with resin 9, and the semiconductor device shown in drawing 1 - drawing 3 is completed.
[0061] Since according to the manufacture method of the semiconductor device of the gestalt this operation it becomes easy to impress the current for electrolysis plating, and the wiring 12 for gold plate is covered by the resist 13 and electrolysis plating is performed in order to connect all main conductive-layer 5e of wiring 5 with the wiring 12 for gold plate and to consider as one pattern, it becomes that it is possible to gold-plate only on the front face of main conductive-layer 5e. Consequently, in the etching process at the time of **********ing the wiring 12 for gold plate and forming wiring 5, 5f of deposits can be used as a mask, and it becomes possible to perform the formation process of wiring 5 simple.
[0062] In addition, without forming the wiring 12 for gold plate in the above-mentioned manufacture method, the pattern of main conductive-layer 5e which is equivalent to the pattern of wiring 5 at once is formed, after that, 5f of deposits which consist of gold plate by electroless deposition may be formed, and wiring 5 may be formed.
[0063] (Gestalt 2 of operation) Drawing 12 is the plan showing the wiring portion of the semiconductor device which is the gestalt of other operations of this invention, and drawing 13 is a XIII-XIII line cross section in drawing 12 .
[0064] The wiring connection 3 by which the semiconductor device of the gestalt 2 of this operation was formed on the semiconductor chip 1 is arranged to the edge field of a semiconductor chip 1, and inner lead section 5b therefore connected to the wiring connection 3 is also arranged by **** of the tape substrate 2 corresponding to it. In such a case, common wiring section 5c can be arranged in the center section of the tape substrate 2, and it can be connected to inner lead section 5b which corresponds directly, without going via land 5a for external electrodes in the wiring connection 3 which should be held from common wiring section 5c to grounding potential or power supply potential. Therefore, the same effect as the gestalt 1 of operation can be acquired. Common wiring section 5c may be not only the shape of a rectangle but a rectangle, a wave, a saw form, or a curve.
[0065] in addition, land 5for external electrodes a, 5d of lead wiring sections, a bump 6, and connection -- since the hole 7, the glue line 8, and the resin 9 grade are the same as that of the gestalt 1 of operation, explanation is omitted Suppose that the manufacture method is the same as that of the gestalt 1 of operation. In addition, in the case of the gestalt 2 of this operation, tape opening is not prepared.
[0066] (Gestalt 3 of operation) Drawing 14 is the plan showing the wiring portion of the semiconductor device of this invention which is the gestalt of other operations further, and drawing 15 is a XV-XV line cross section in drawing 14 .
[0067] As for the semiconductor device of the gestalt 3 of this operation, it has two tape substrates 2 by cutting the tape substrate 2 in the center section of the semiconductor chip 1, and the tape opening 4 is formed in the semiconductor chip 1 central approach of each tape substrate 2. Common wiring section 5c is installed along the semiconductor chip 1 center-section side edge side of each tape substrate 2, and land 5a for external electrodes is arranged on the semiconductor chip 1 outside of each tape substrate 2.
[0068] Also in such a case, it can connect with inner lead section 5b which corresponds directly, without going via land 5a for external electrodes in the wiring connection 3 which should be held from common wiring section 5c to grounding potential or power supply potential, and the same effect as the gestalt 1 of operation can be acquired. The configuration of common wiring section 5c may also be a rectangle which was stated with the gestalten 1 and 2 of the aforementioned implementation, a wave, a saw form, or a curve.
[0069] in addition, 5d of lead wiring sections, a bump 6, and connection -- since the hole 7, the glue line 8, and the resin 9 grade are the same as that of the gestalt 1 of operation, explanation is omitted Suppose that the manufacture method is the same as that of the gestalt 1 of operation.
[0070] Moreover, when it has the tape substrate 2 divided into two like the gestalt 3 of this operation, as shown in drawing 16 and drawing 17 , it is possible to form the field of common wiring section 5c of the tape substrate 2 in piles. Drawing 16 is the plan showing the wiring portion of other examples of the semiconductor device of this invention which is the gestalt of other operations further, and drawing 17 is a XVII-XVII line cross section in drawing 16 . In such a case, in order to form

common wiring section 5c of the tape substrate 2 in piles, it becomes possible to reduce the area occupied by the tape substrate 2 whole, and it becomes possible to attain the miniaturization of a semiconductor device.
[0071] As mentioned above, although invention made by this invention person was concretely explained based on the gestalt of implementation of invention, it cannot be overemphasized by this invention that it can change variously in the range which is not limited to the gestalt of the aforementioned implementation and does not deviate from the summary.
[0072] For example, although you may be other organic system material although the case of a polyimide was illustrated for the tape substrate 2 with the gestalt of this operation, and a bump's 6 quality of the material was used as solder, it cannot be overemphasized that you may be a golden bump.

[Translation done.]

* NOTICES *

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is the perspective diagram having shown an example of the appearance of the semiconductor device which is the gestalt of 1 operation of this invention.
[Drawing 2] It is the plan showing the wiring portion of the semiconductor device shown in drawing 1 .
[Drawing 3] III-III in drawing 1 and drawing 2 It is a line cross section.
[Drawing 4] An example of the manufacture method of the semiconductor device of the gestalt 1 of operation is shown in order of the process, (a) is a bottom plan view and (b) is a b-b line cross section in (a).
[Drawing 5] An example of the manufacture method of the semiconductor device of the gestalt 1 of operation is shown in order of the process, (a) is a bottom plan view and (b) is a b-b line cross section in (a).
[Drawing 6] An example of the manufacture method of the semiconductor device of the gestalt 1 of operation is shown in order of the process, (a) is a bottom plan view and a b-b line cross section [in / (a) / in (b)] and (c) are the cross sections having shown an example of the manufacture method of a semiconductor device in order of the process.
[Drawing 7] An example of the manufacture method of the semiconductor device of the gestalt 1 of operation is shown in order of the process, (a) is a bottom plan view and (b) is a b-b line cross section in (a).
[Drawing 8] An example of the manufacture method of the semiconductor device of the gestalt 1 of operation is shown in order of the process, (a) is a bottom plan view and (b) is a b-b line cross section in (a).
[Drawing 9] An example of the manufacture method of the semiconductor device of the gestalt 1 of operation is shown in order of the process, (a) is a bottom plan view and a b-b line cross section [in / (a) / in (b)] and (c) are the cross sections having shown an example of the manufacture method of a semiconductor device in order of the process.
[Drawing 10] It is the cross section having shown an example of the manufacture method of the semiconductor device of the gestalt 1 of operation in order of the process.
[Drawing 11] It is the cross section having shown an example of the manufacture method of the semiconductor device of the gestalt 1 of operation in order of the process.
[Drawing 12] It is the plan showing the wiring portion of the semiconductor device which is the gestalt of other operations of this invention.
[Drawing 13] It is a XIII-XIII line cross section in drawing 12 .
[Drawing 14] It is the plan showing the wiring portion of the semiconductor device of this invention which is the gestalt of other operations further.
[Drawing 15] It is a XV-XV line cross section in drawing 14 .
[Drawing 16] It is the plan showing the wiring portion of other examples of the semiconductor device of this invention which is the gestalt of other operations further.
[Drawing 17] It is a XVII-XVII line cross section in drawing 16 .
[Description of Notations]
1 Semiconductor Chip
2 Tape Substrate
3 Wiring Connection
4 Tape Opening
5 Wiring
5a The land for external electrodes
5a-1 Grounding external electrode land
5a-2 Power supply external electrode land
5b Inner lead section
5c Common wiring section
5c-1 Grounding common wiring
5c-2 Power supply common wiring
5d Lead wiring section
5d-1 Grounding lead wiring
5d-2 Power supply lead wiring
5d-3 Grounding lead wiring
5d-4 Power supply lead wiring
5e The main conductive layer
5f Deposit
6 Bump
7 Connection -- Hole
8 Glue Line
9 Resin
10 Polyimide Tape

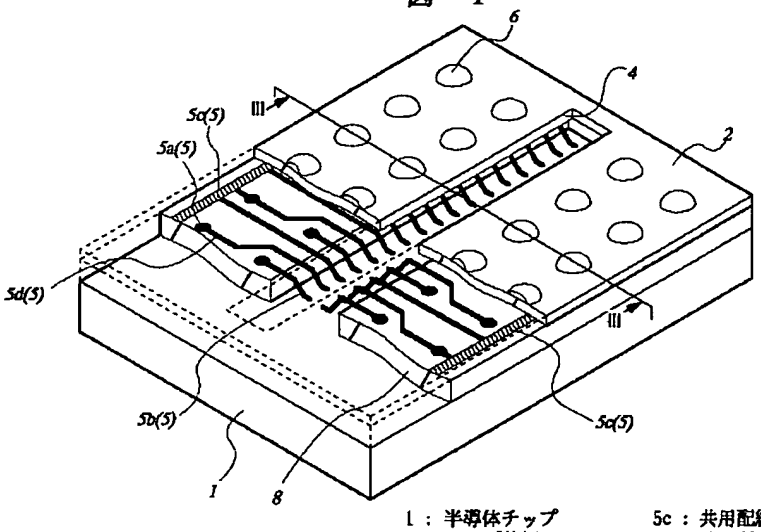
11 Thin Film
12 Wiring for Gold Plate
13 Resist
14 Tool

[Translation done.]

DRAWINGS

[Drawing 1]

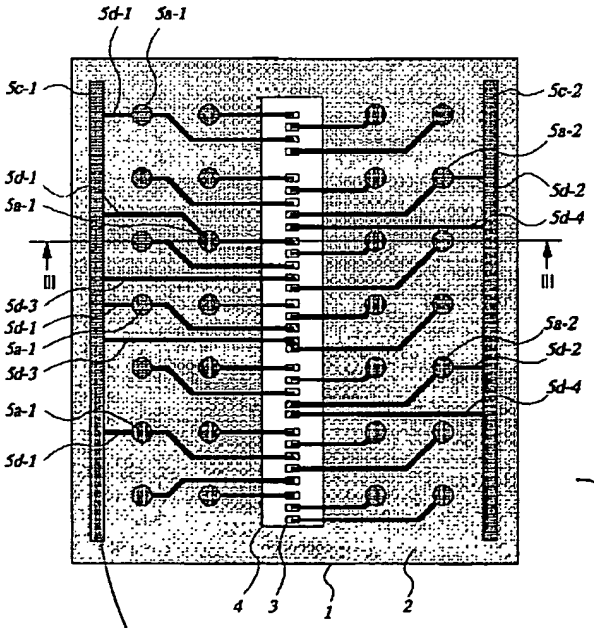
図 1

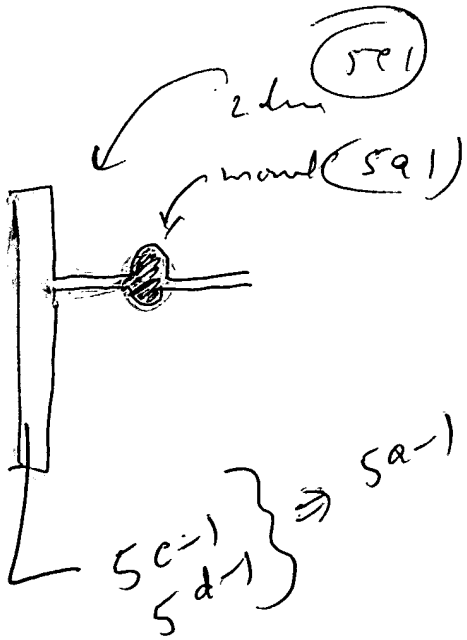


1 : 半導体チップ
2 : テープ基板
5 : 配線
5a : 外部電極用ランド部
5b : インナーリード部
5c : 共用配線部
5d : リード配線部
8 : 接着層

[Drawing 2]

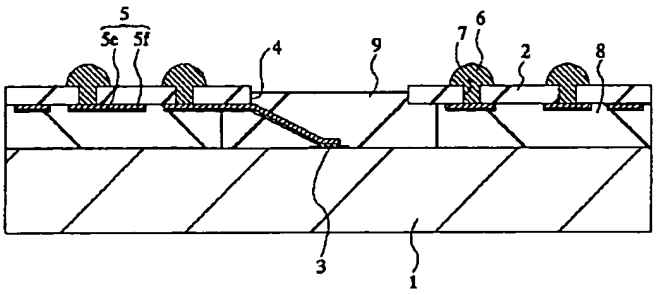
図 2





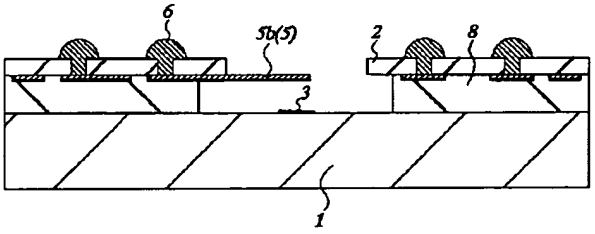
[Drawing 3]

図 3



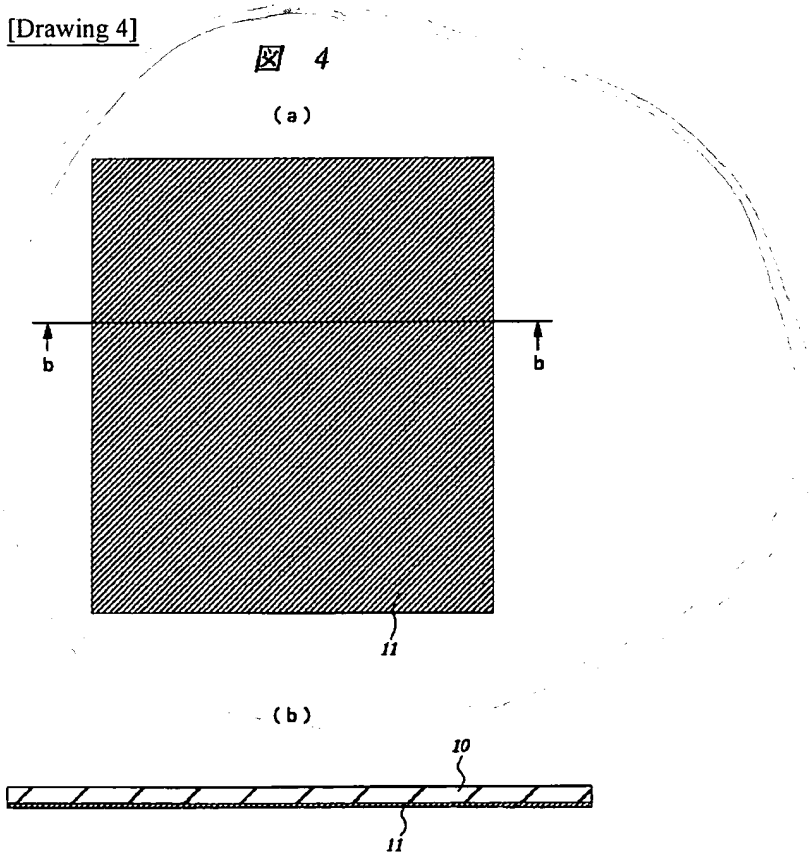
[Drawing 10]

図 10



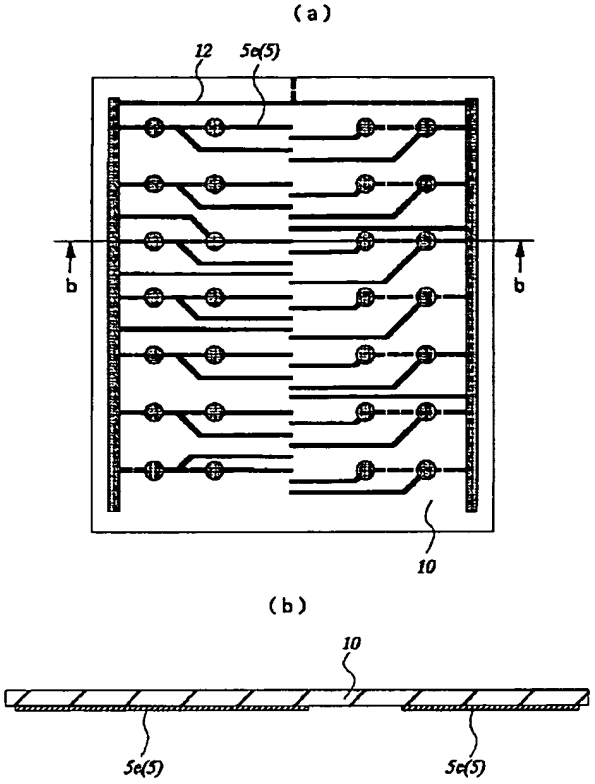
[Drawing 4]

図 4



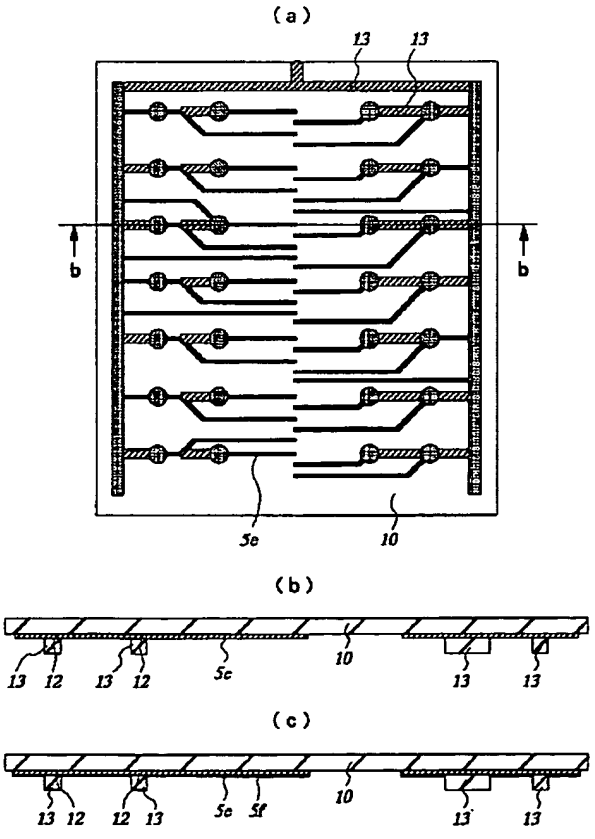
[Drawing 5]

図 5



[Drawing 6]

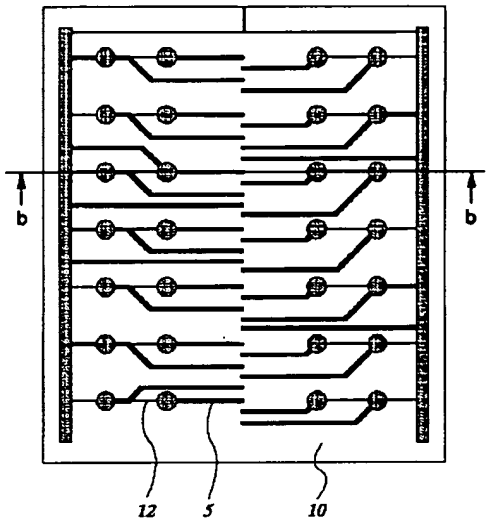
図 6



[Drawing 7]

図 7

(a)



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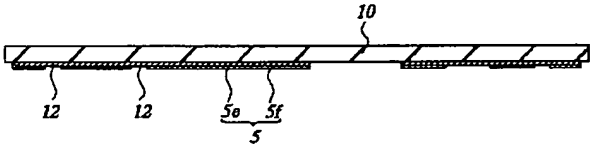
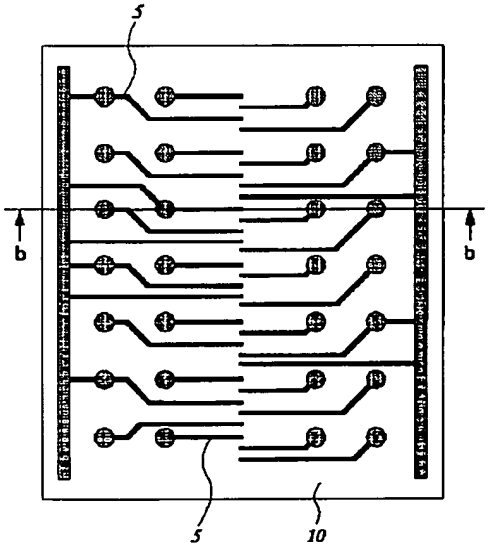


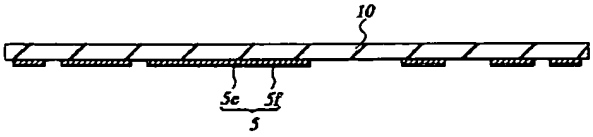
[Drawing 8]

図 8

(a)

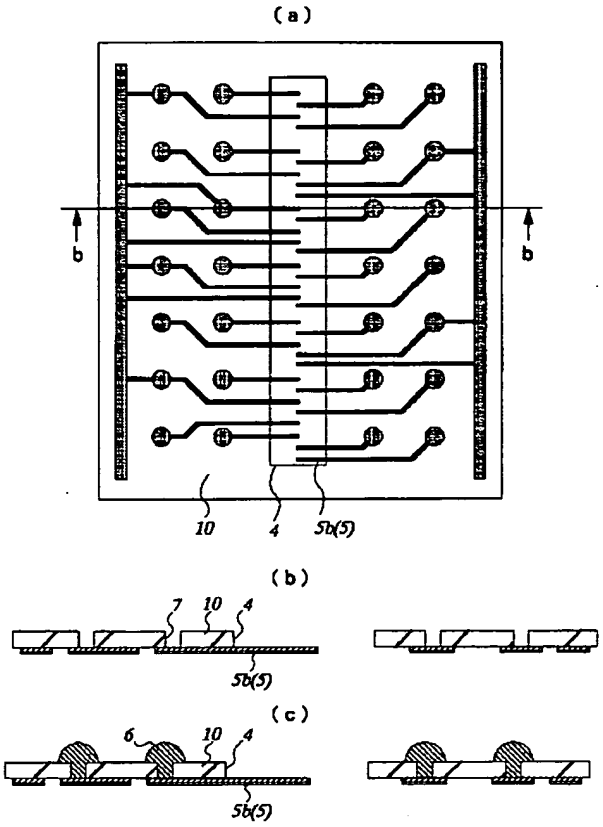


(b)



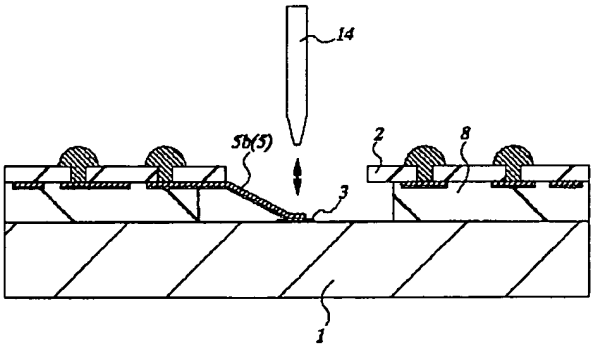
[Drawing 9]

図 9



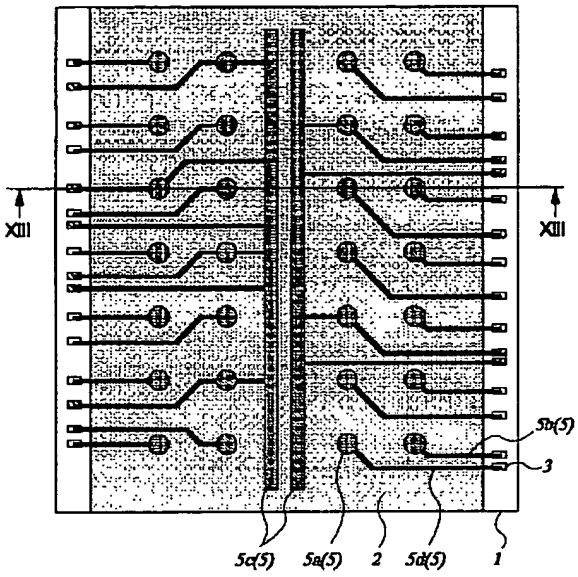
[Drawing 11]

図 11



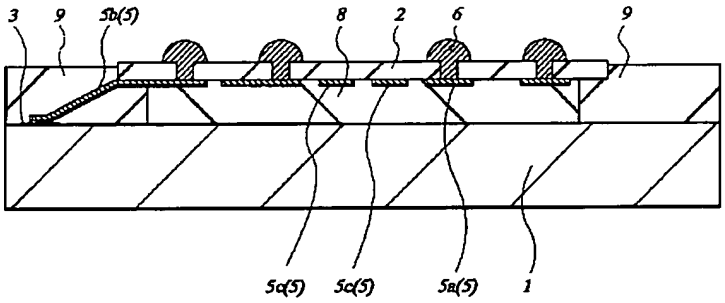
[Drawing 12]

図 1 2



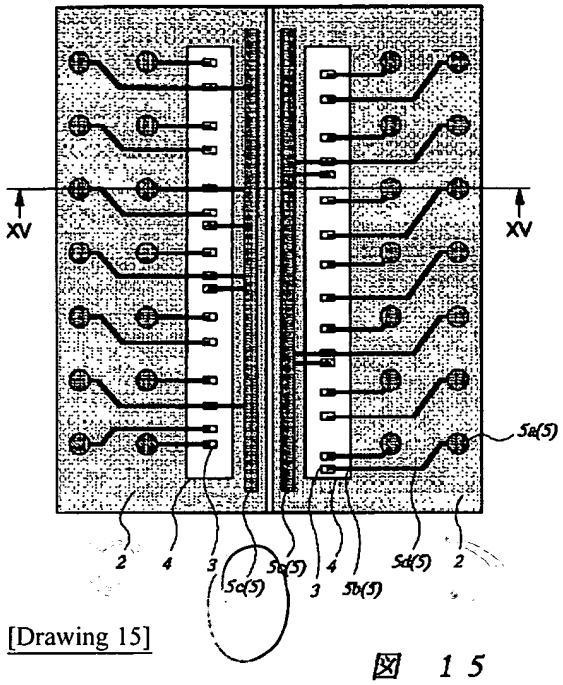
[Drawing 13]

図 1 3



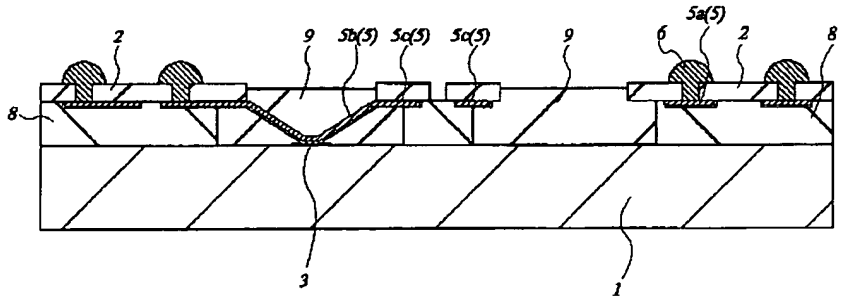
[Drawing 14]

図 14



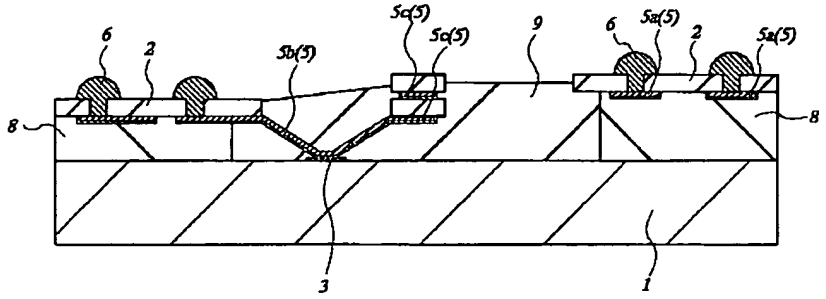
[Drawing 15]

図 15



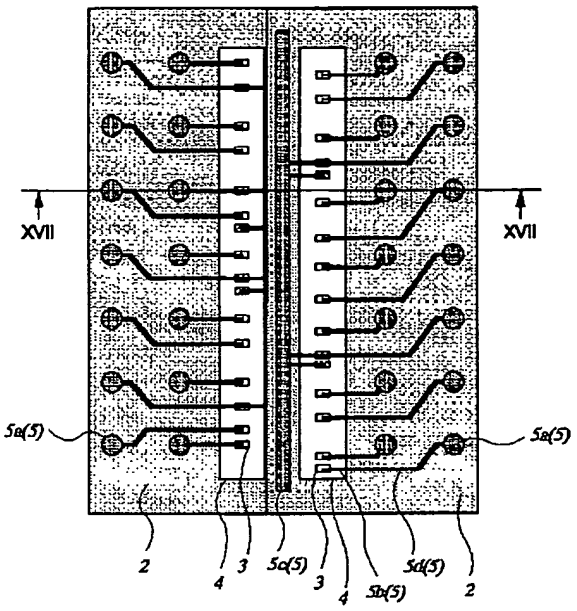
[Drawing 17]

図 17



[Drawing 16]

図 16



[Translation done.]